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ECE 546

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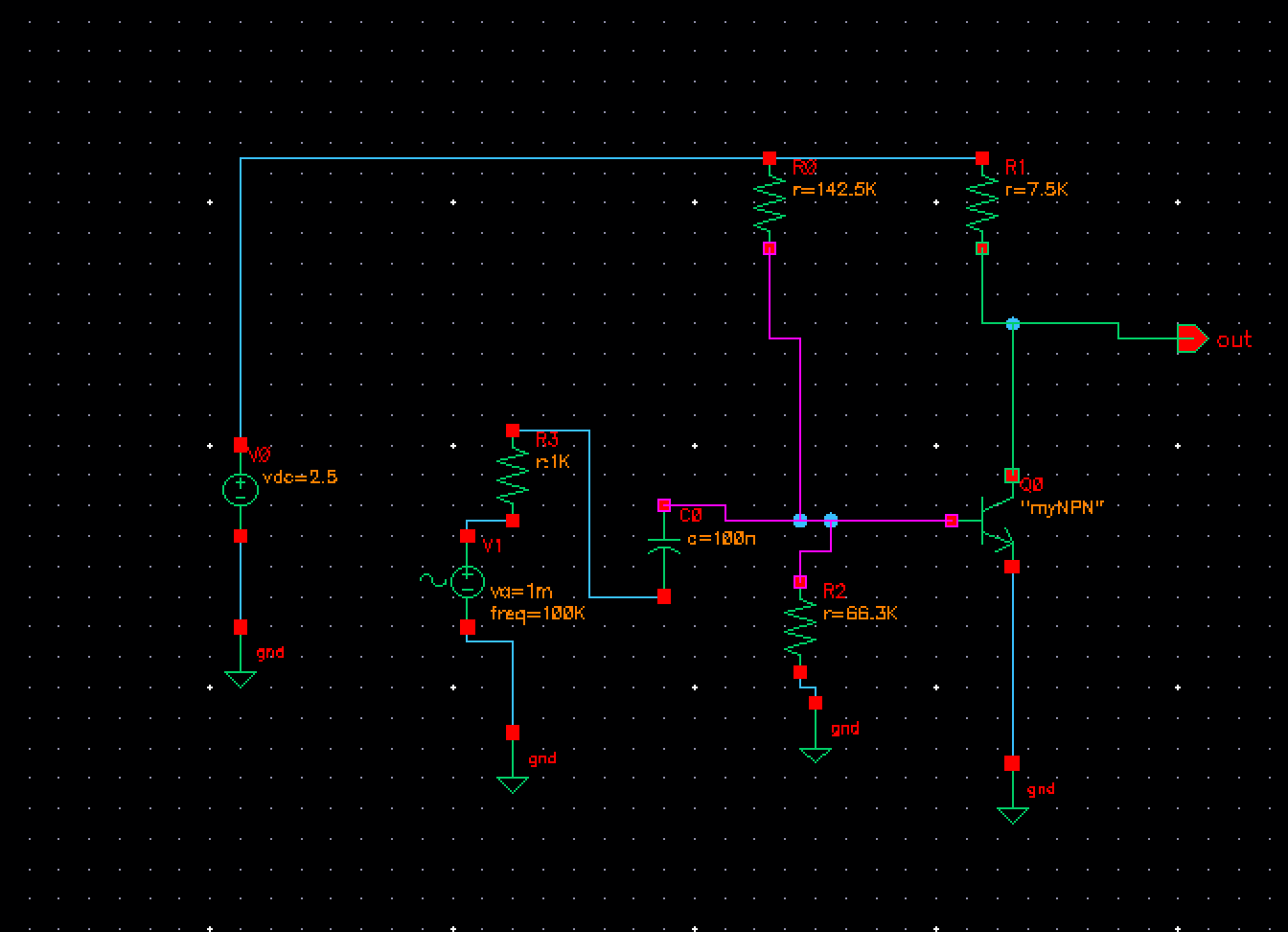
9-27-20

**ECE 546 LAB1 Report**

Task #1: Common Emmitter and Amplifier (CE&A)

Part1: Drawing of the schematic circuit of the CE and Amplifier using the *mynpn* device module given from the instructor.

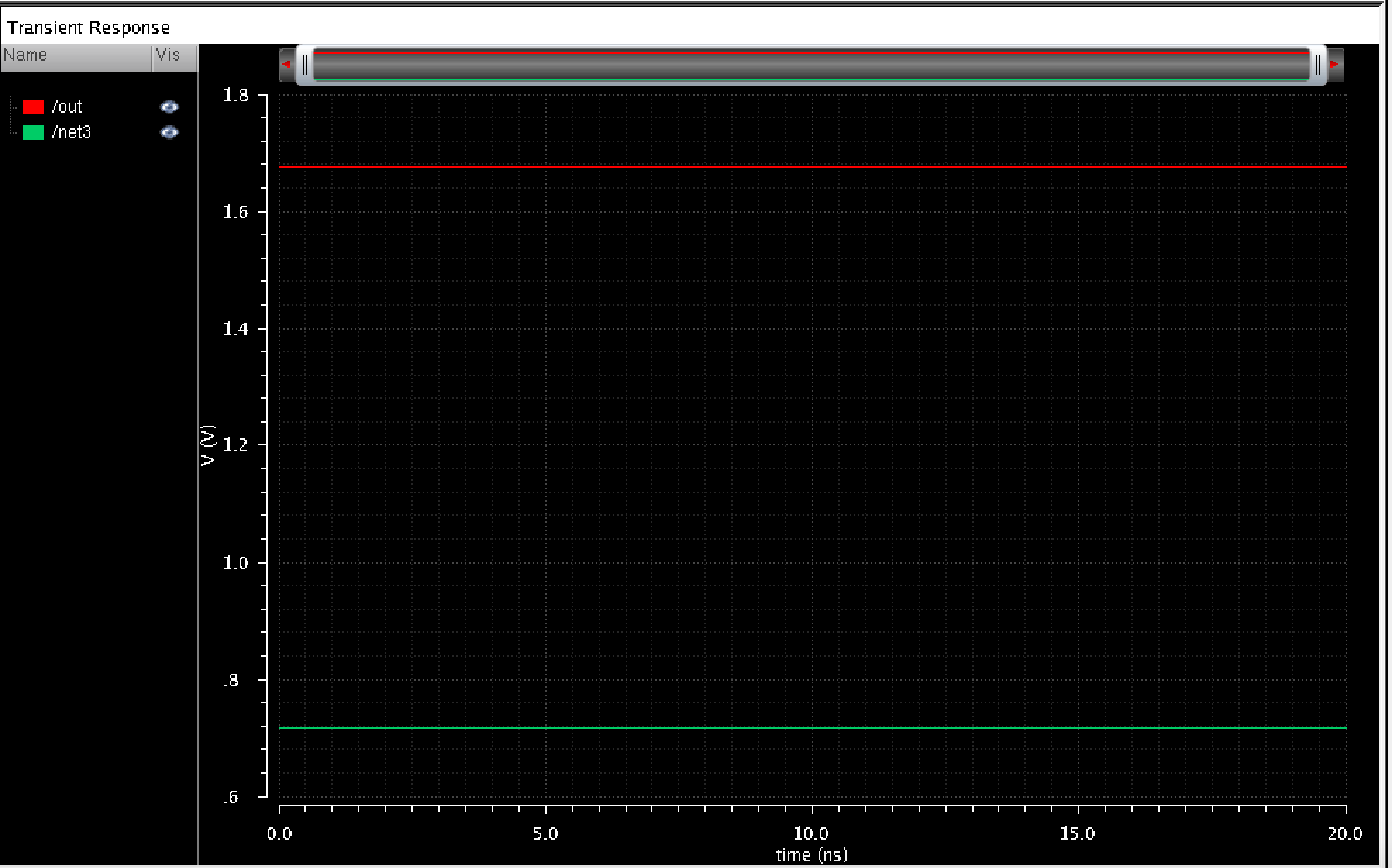
**Schematic of the CE&A Circuit shown below:**



*Description: This circuit demonstrates the schematics of the common emitter along with two amplifiers using the “myNPN” transistor given in order to observe a proper behavior analog analysis using the myNPN.*

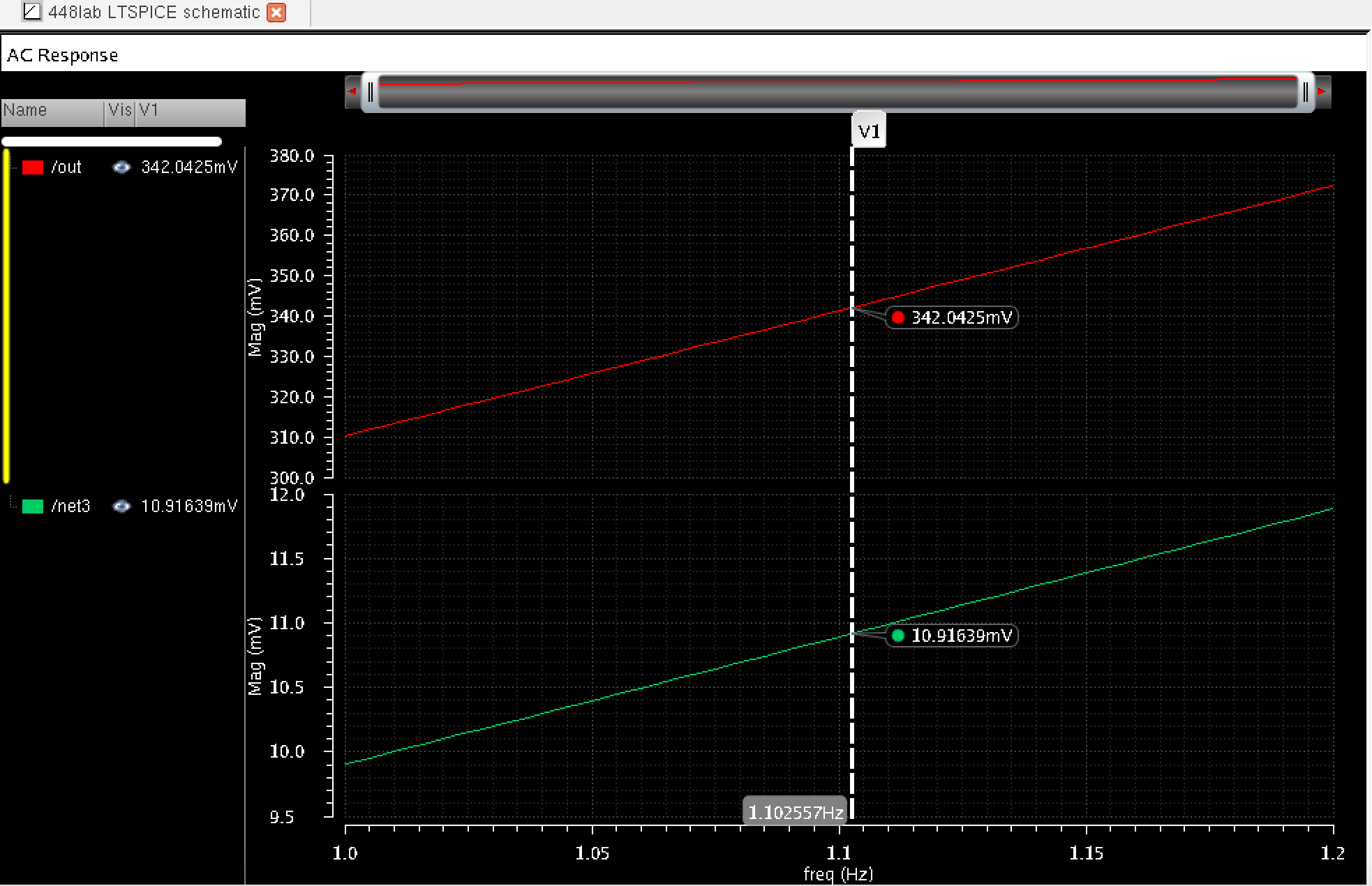
Part2: Comparing both performances of the Trasient and AC Analysis gain and circuit output.

**The Transient Amplifier behavior figure shown below:**

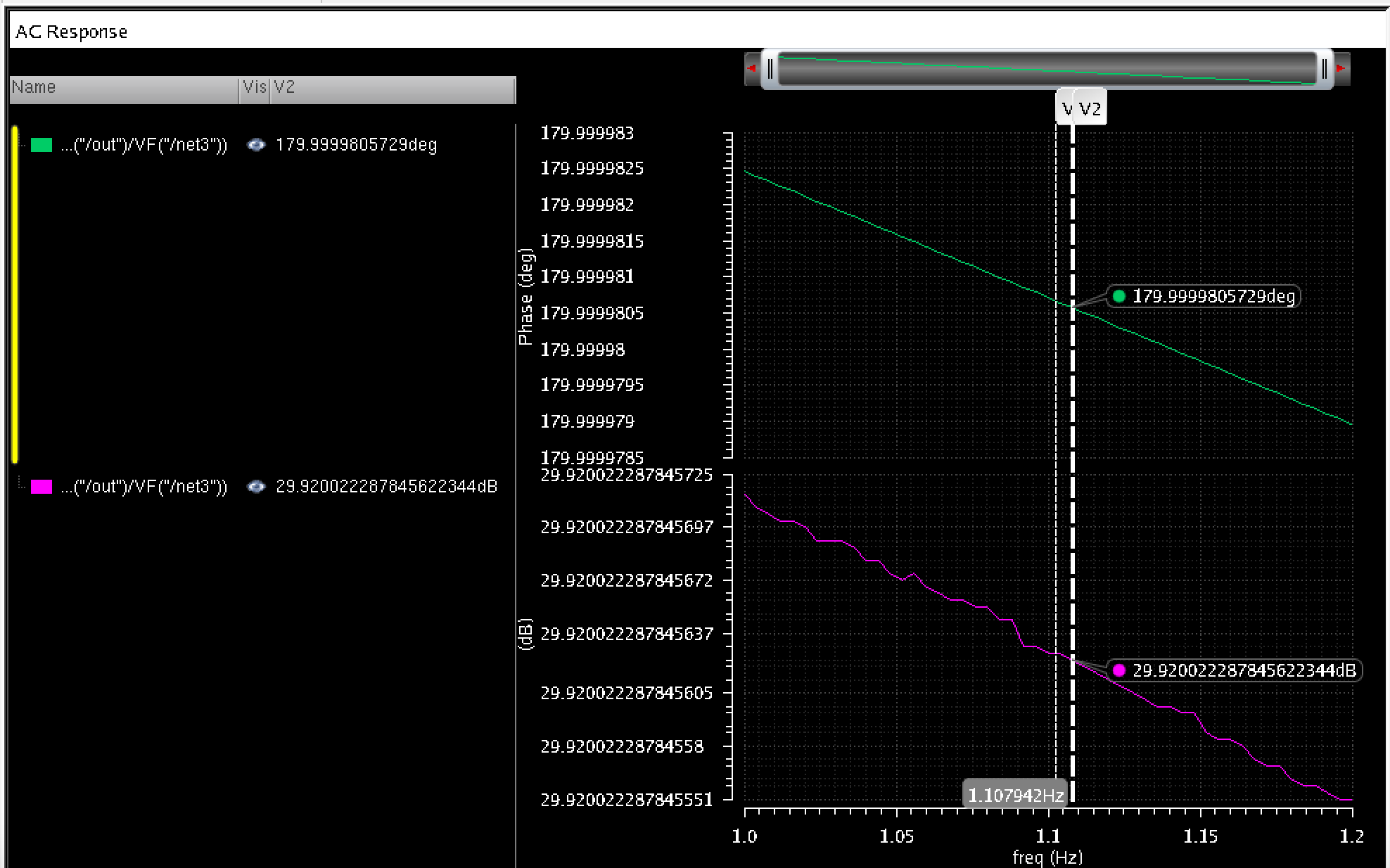


Description: The graphs contains the results of the input/output gain of the transient. The output is displayed as red, as well as the gain is displayed as green. Both assets contain a constant signal frequency that is stunted. Thus results in no changes within the circuits behavior.

**AC analysis of the Transient Amplifier shown below:**

Description: The output and net voltage rates of the transient amplifier is parallel as signal frequency increases through the Capacitor emitter along with the increase of the voltage sources.

**Analytical Behavior of the Gain during AC Response**

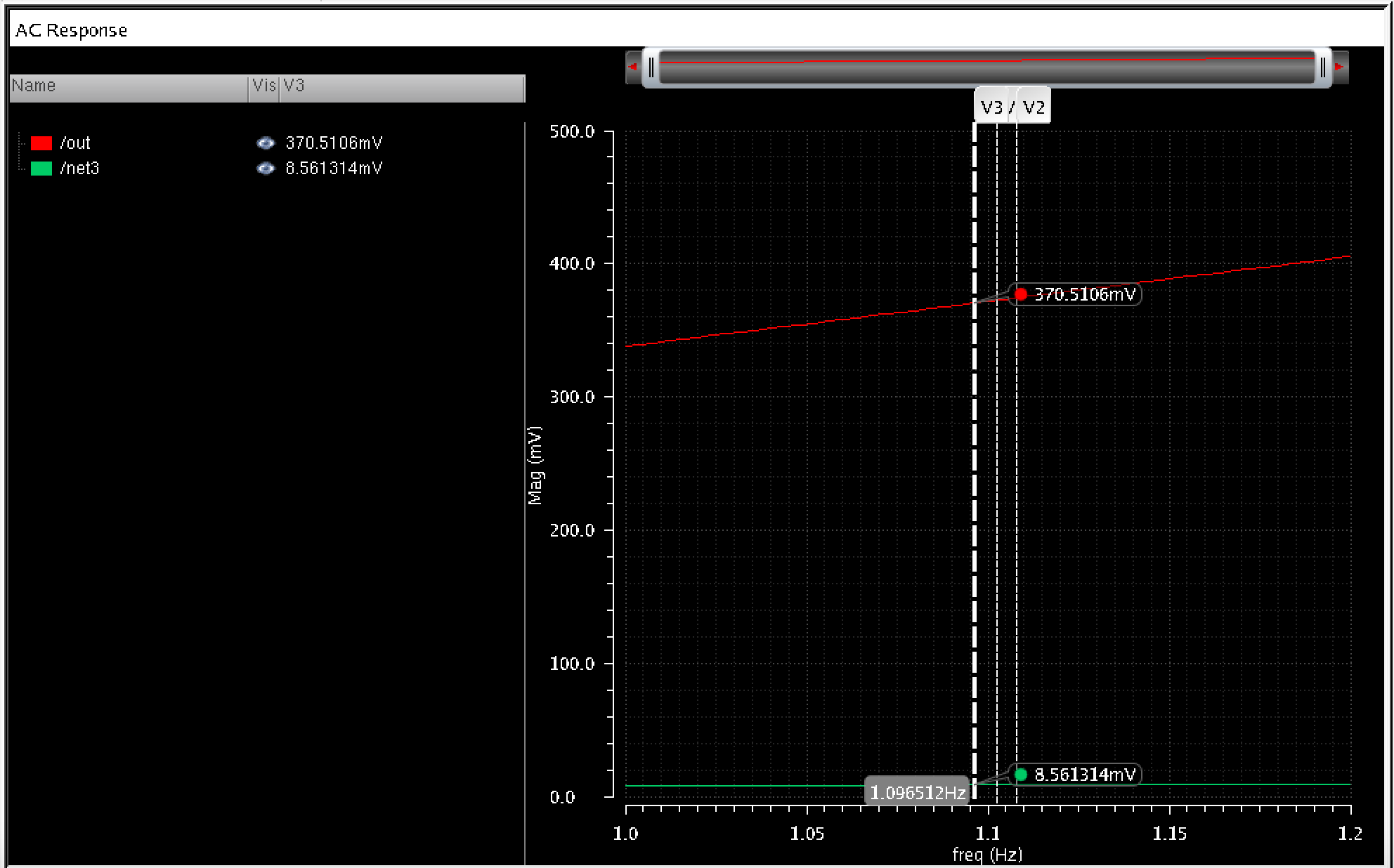
Description: After performing both transient and AC analysis to compare similar gain and phase degeneration, we obtained a more accurate result that is similar to the gain in slide 37.

Part3: Performance of the DC sweep for V1 dc voltage in order to find the DC value such that the output DC value is 600mV

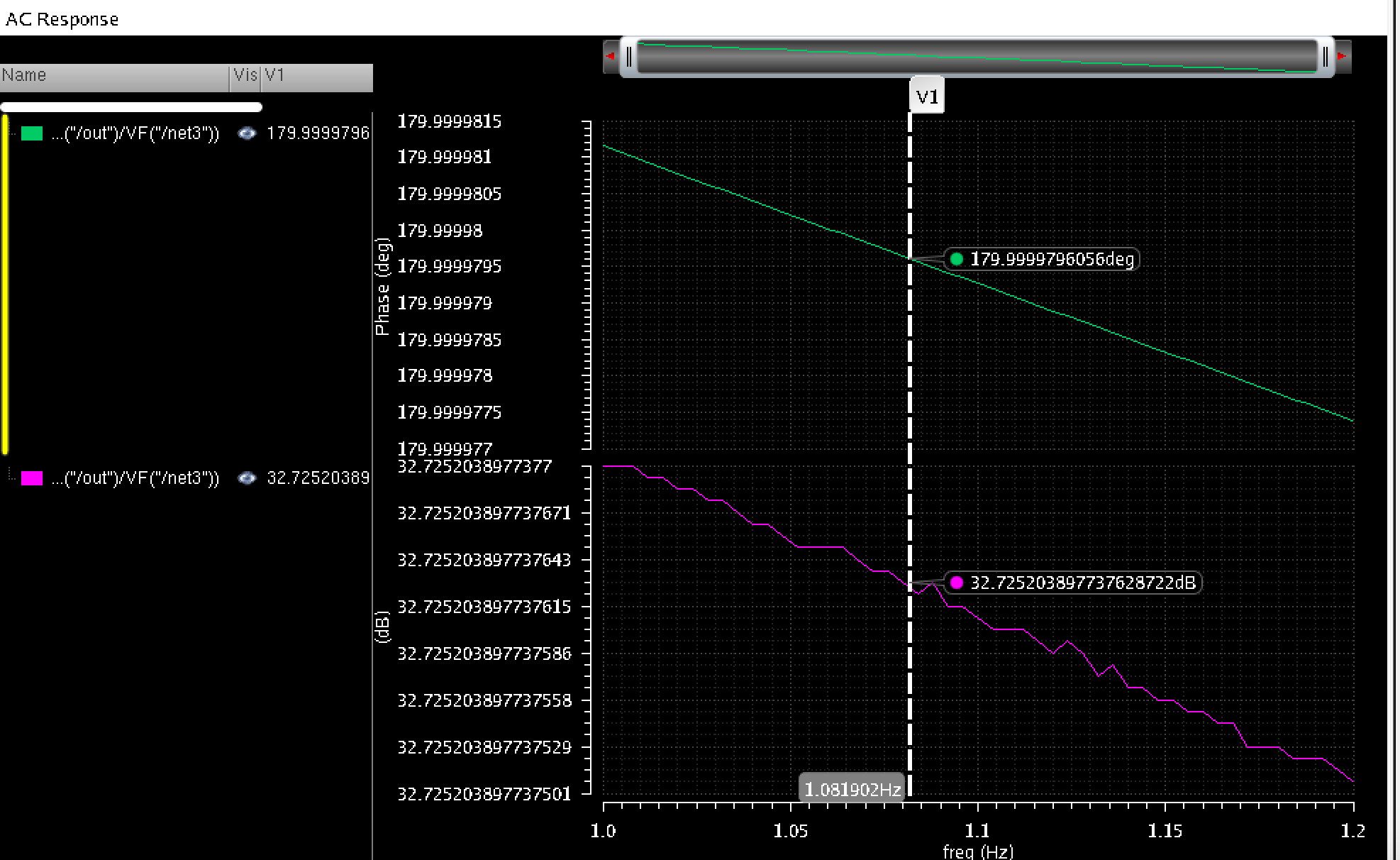
Interpretation:

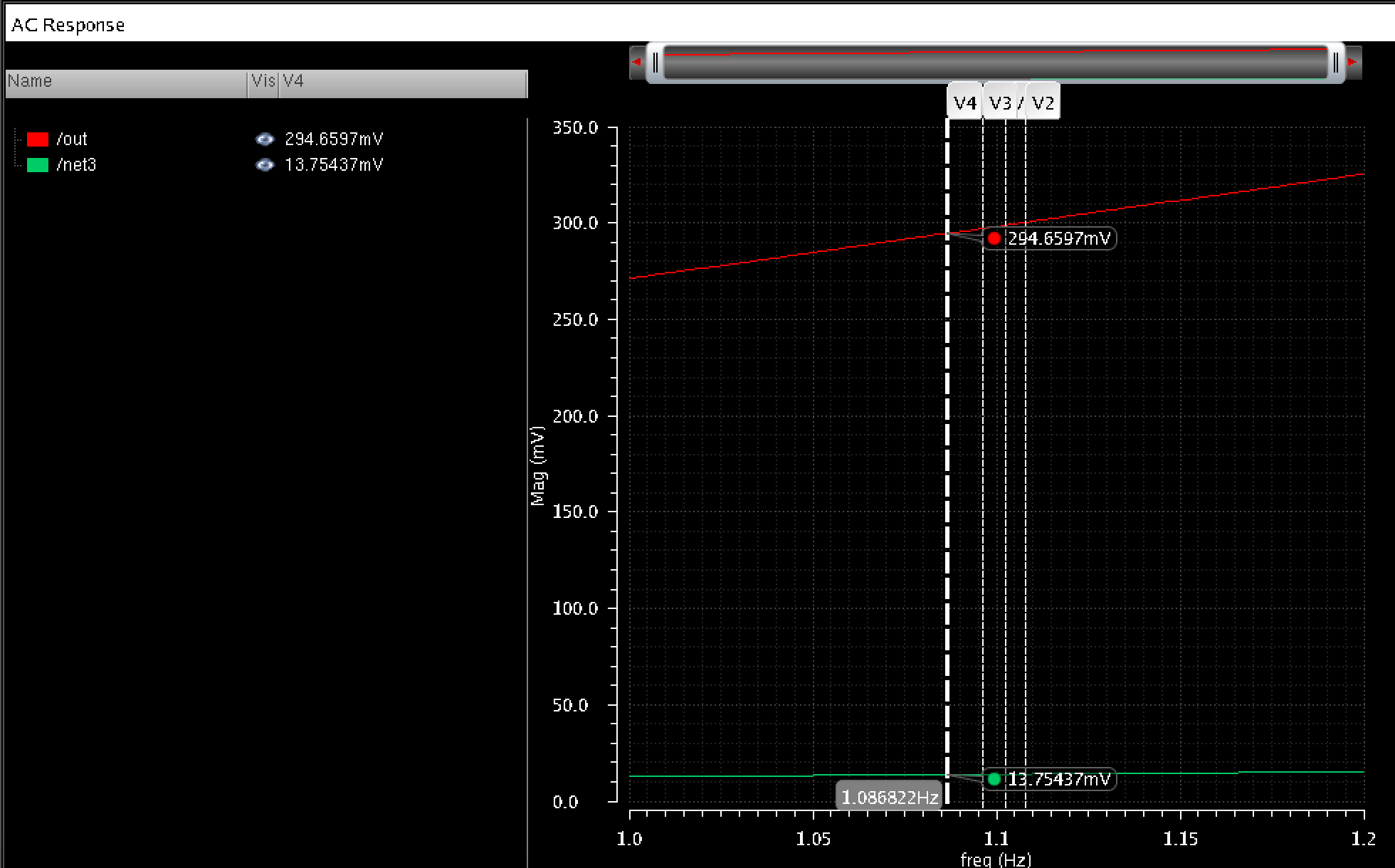
By using parametric analysis methods to obtain the amplifier gain and signal ground level at the output, we acknowledge that if R1 vary either from +5% or -5%, there is a slightly different result. For -5% (R=142.5k ohm), we discovered that the gain has increased. Results are displayed below:

**AC Analysis of the gain and output at -5% (R=142.5Kohm) below:**

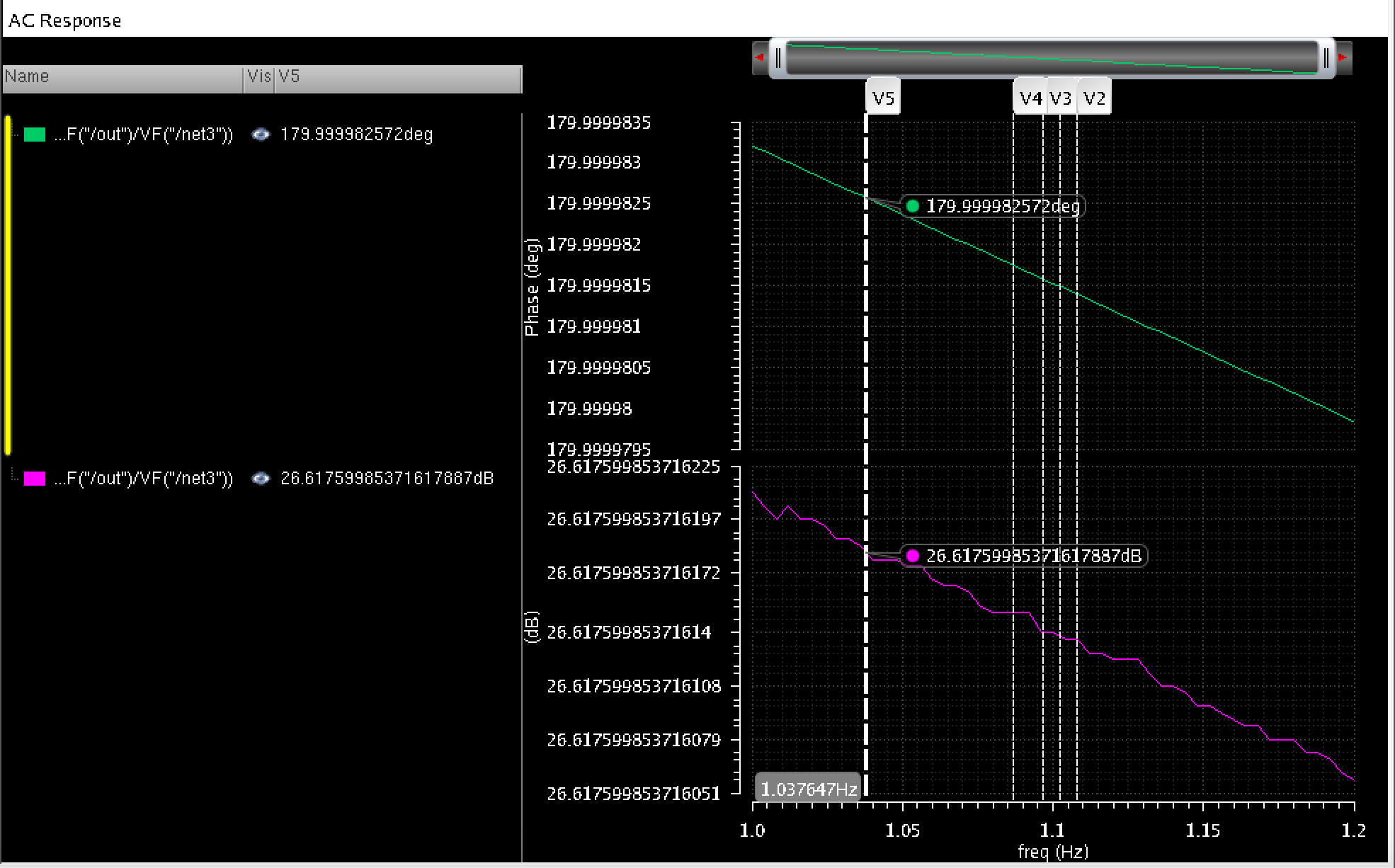
Description: After results are conducted, we discovered that the magnitude within voltage of the gain and output amplifier increases as the resistance for R1 decreases by %5.

**The Gain and Phase of the Amplifier at -5% (R=142.5Kohm) as below:**

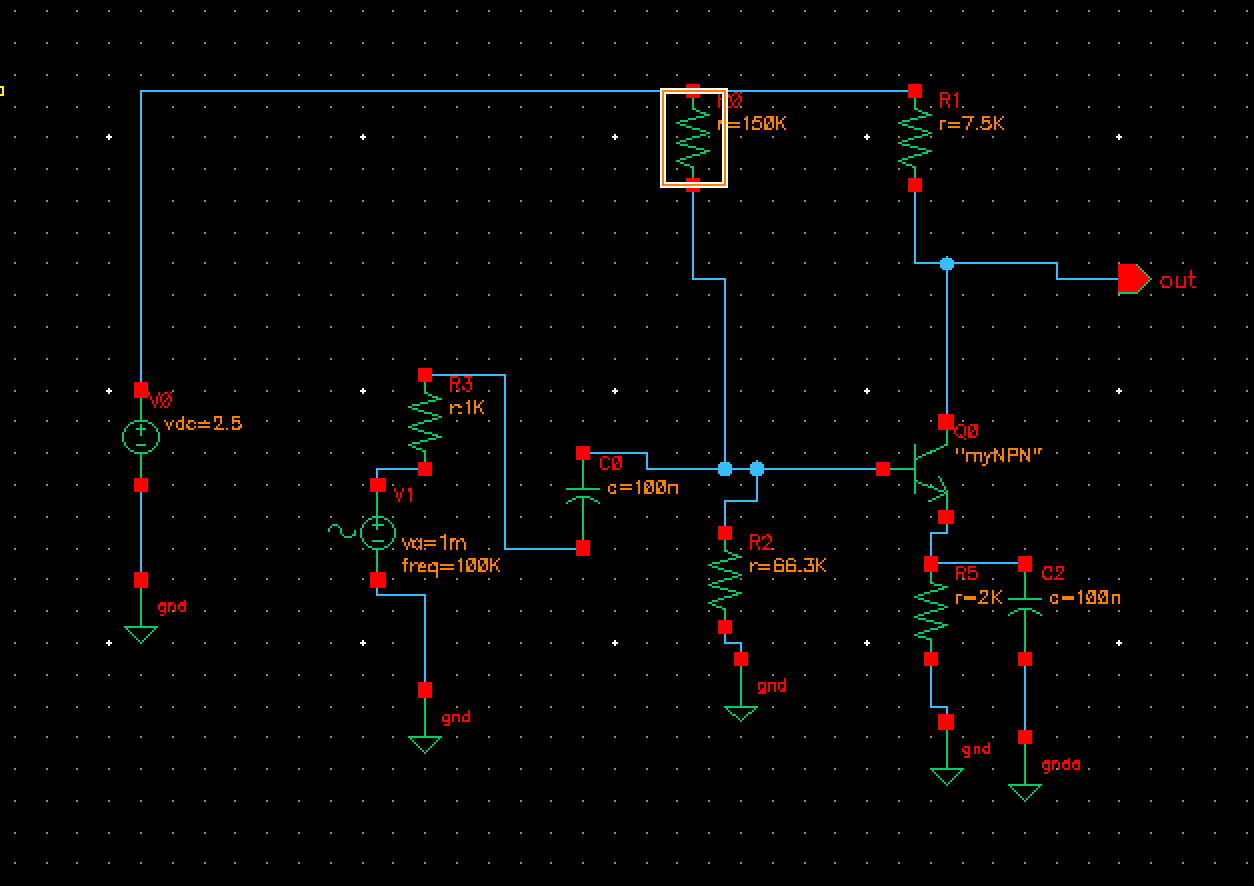
Description: The gain and phase of the amplifier frequency, however, decreases drastically as R1 is decreased by %5.

**AC Analysis of the gain and signal output of the Amplifier at +5% (157.5K OHM)** Description: As shown in the results above for the +5% (R= 157.5K OHM), we have received the opposite results in which the gain has decreased a little bit as introduced in the previous figure above.

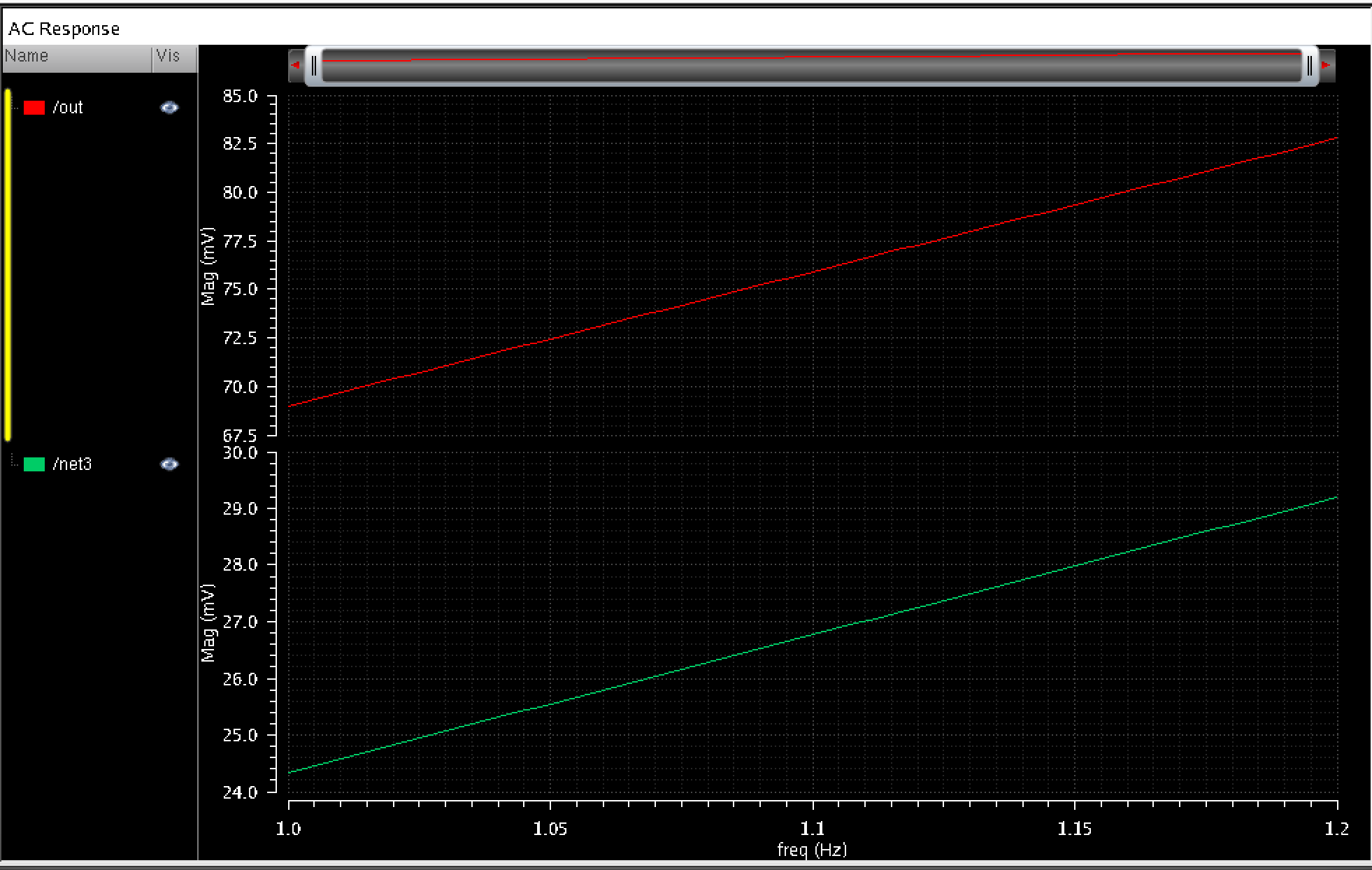
**The Gain and Phase of the Amplifier at +5% (157.5K OHM)**

Description: As the resistance in R1 increases by 5%, which is R1 = 150Ω\*0.05 = 7.5, the original ohms of R1 results to R1 = 157.5Ω. At this rate for the resistance, the frequency signal of the gain and phase output signal faces a drastic deflation in performance due to the increase in resistor.

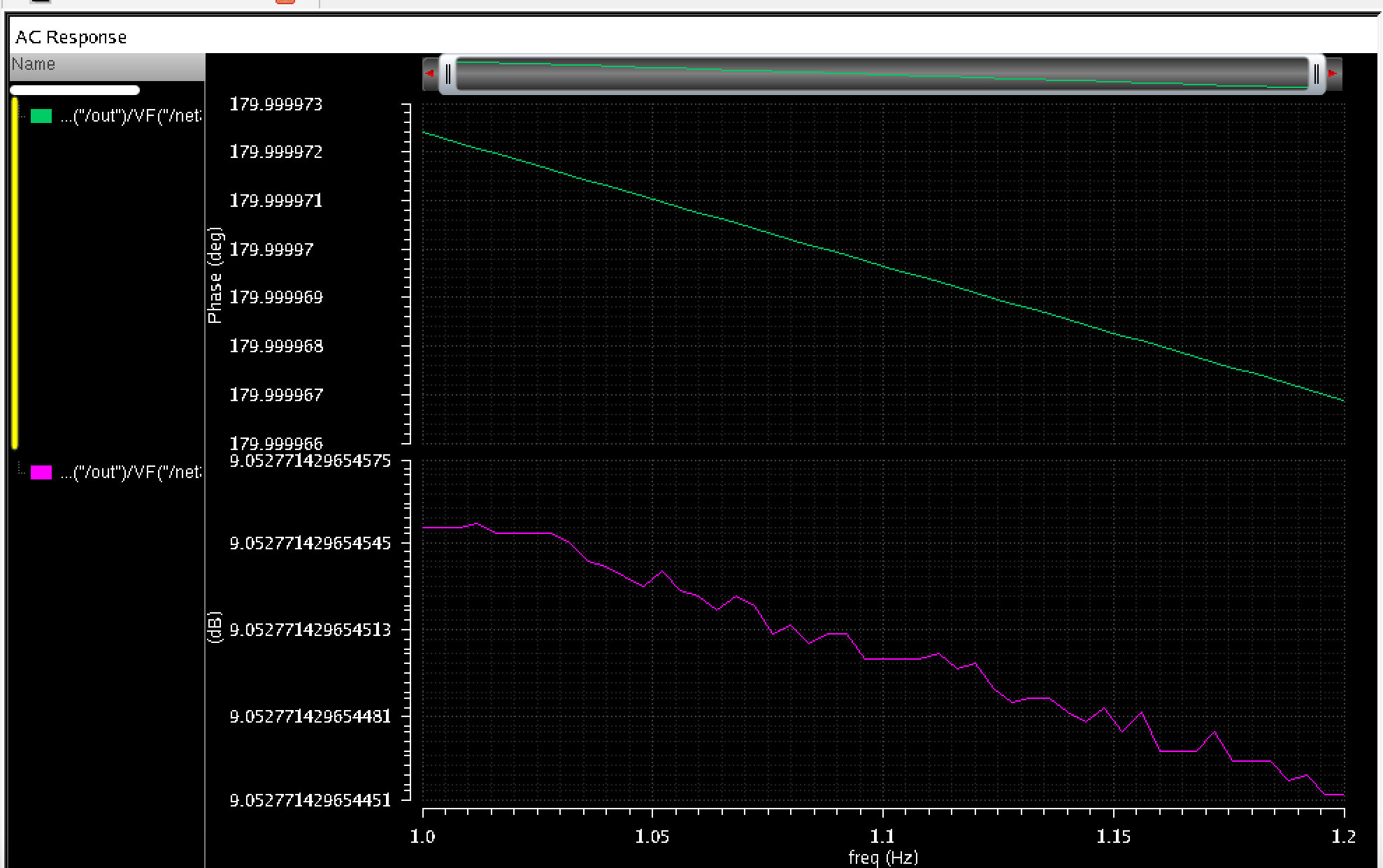
Part4: Modifying the circuit with adding emitter degeneration

**Schematics of the Emitter Degeneration as shown below:**Description: Adding the resister with a capacitor in parallel to the emitter term significantly improves the gain in the circuit. The figure above is a schematic of the new circuit that is similar to the circuit on lecture slide 34.

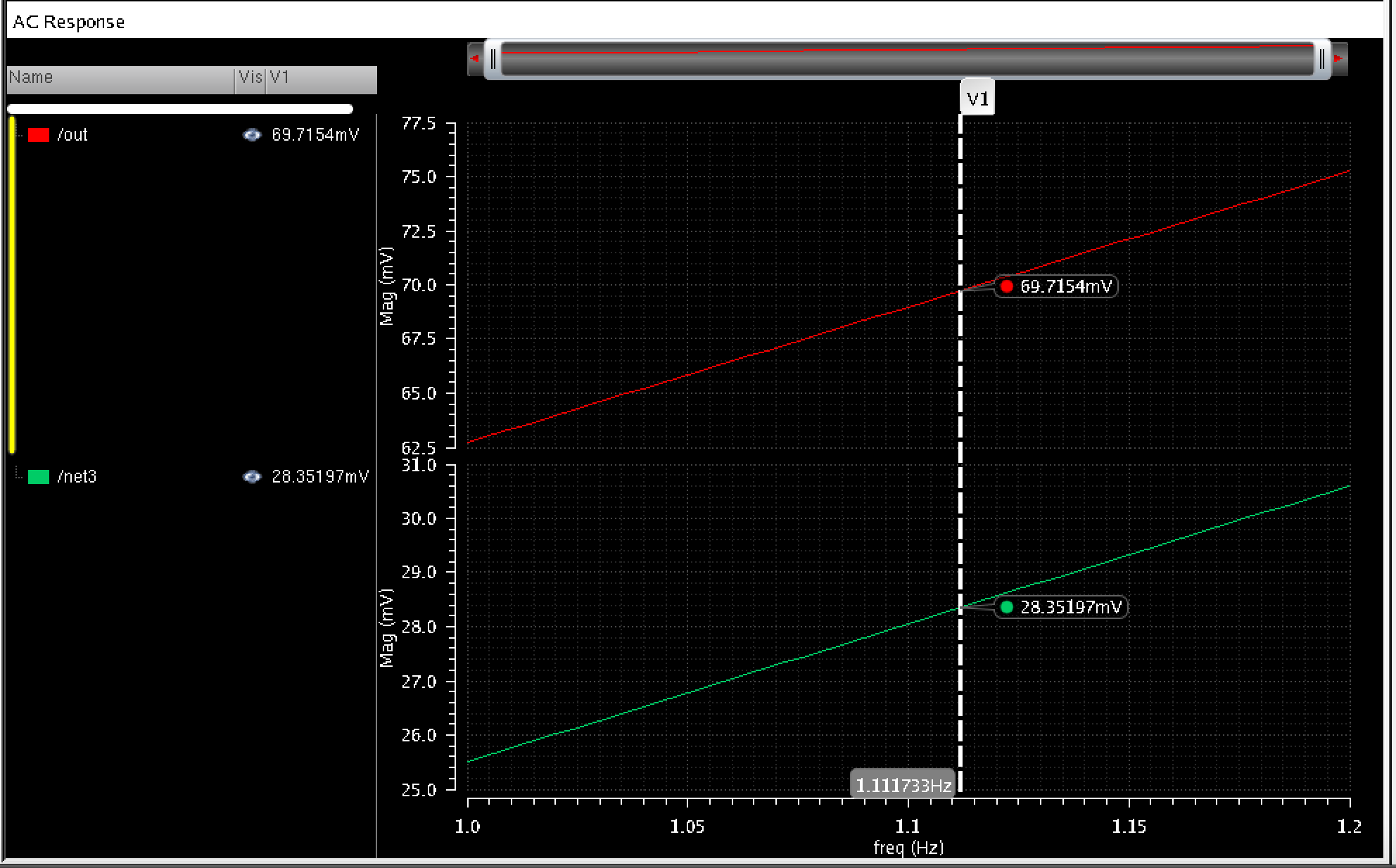
**The R to -5% accelerating to 142.5K ohm as displayed below:**

Description: We performed the AC analysis and discovered that the results for the gain of both negative and positive %5 of R1 have a few slight changes towards the performance. The results are displayed in the figure above.

**The Gain and phase of the Amplifier shown below:**

Description: From our previous tests done by the figures on above, we determined that when the resistor increases by %5, the integration of the frequency of the amplifier’s phase decreases drastically.

**AC analysis of the gain and signal output shown below:**

Description: Updated results to no changes in the gain or signal output of the amplifier

**The Gain and Phase of the amplifier shown below**

Description: When we increased voltage gain through the resistor and the capacitor, the emitter then became an emitter degeneration. As a result, the more resistivity we added, the better the performance of the gain.

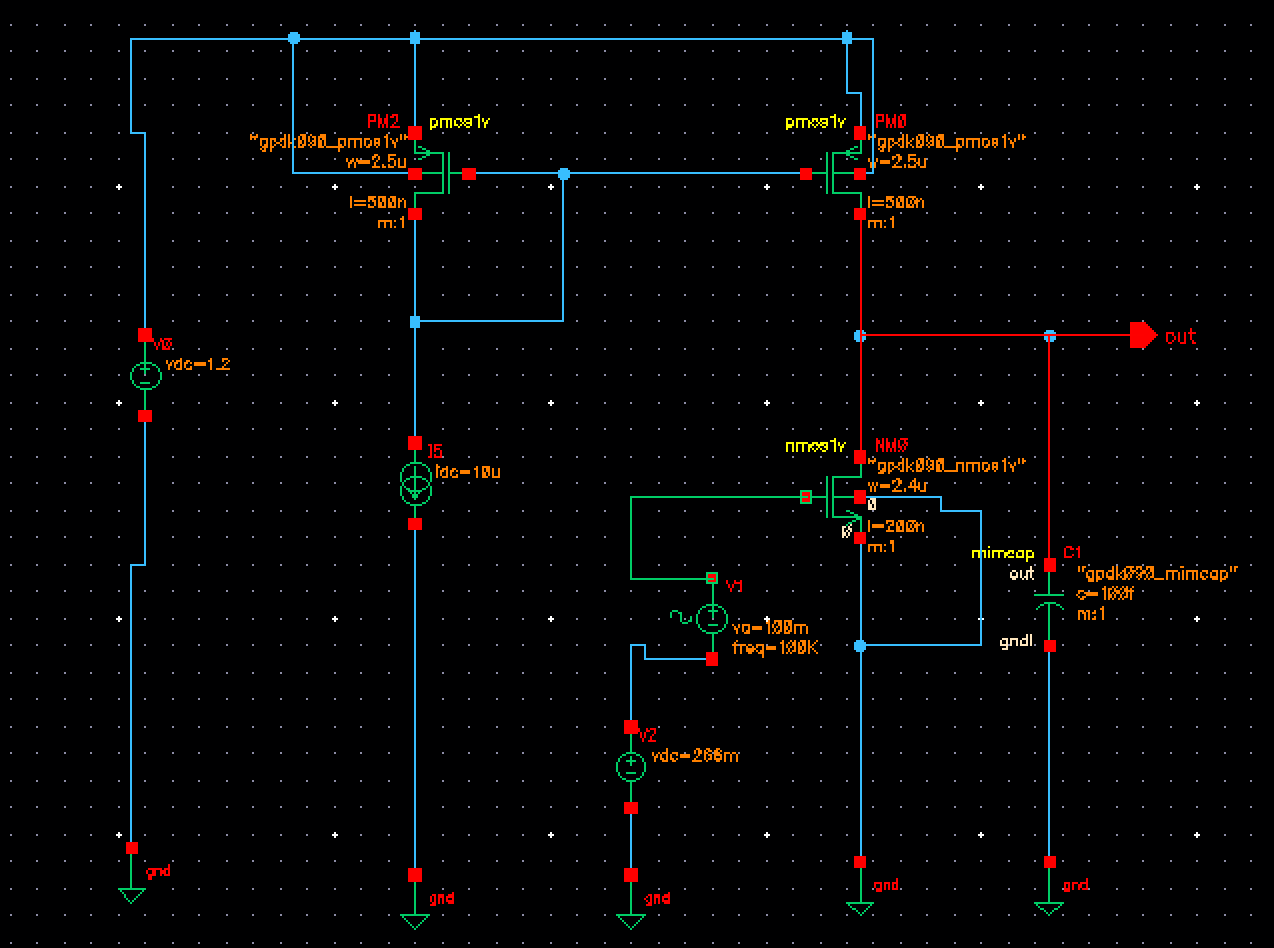
Task#2: Common Source Amplifier Simulation

Part1: Drawing of the schematic in NMOS using DC biasing voltage

Performance:

Here we displayed a drawing of the Schematic, in NMOS(2.4U/200n) that forms a common source amplifier and PMO(2.5u/ 500n) that are both active loads. We used PMO and PM1to form a current mirror circuit in order to provide a biasing voltage for PMO using the reference to the DC current of I4 (10uA). Thus, the DC biasing voltage of NMO is given by the dc value of V1 – which is the vhc component from AnalogLib). Whiling using V2 ( vdc from analoglib) as a AC input, it advocated in amplifying the circuit.

**Schematics of NMOS circuit using DC biasing voltage**



Part2: The DC biasing of NM0 to 600mV

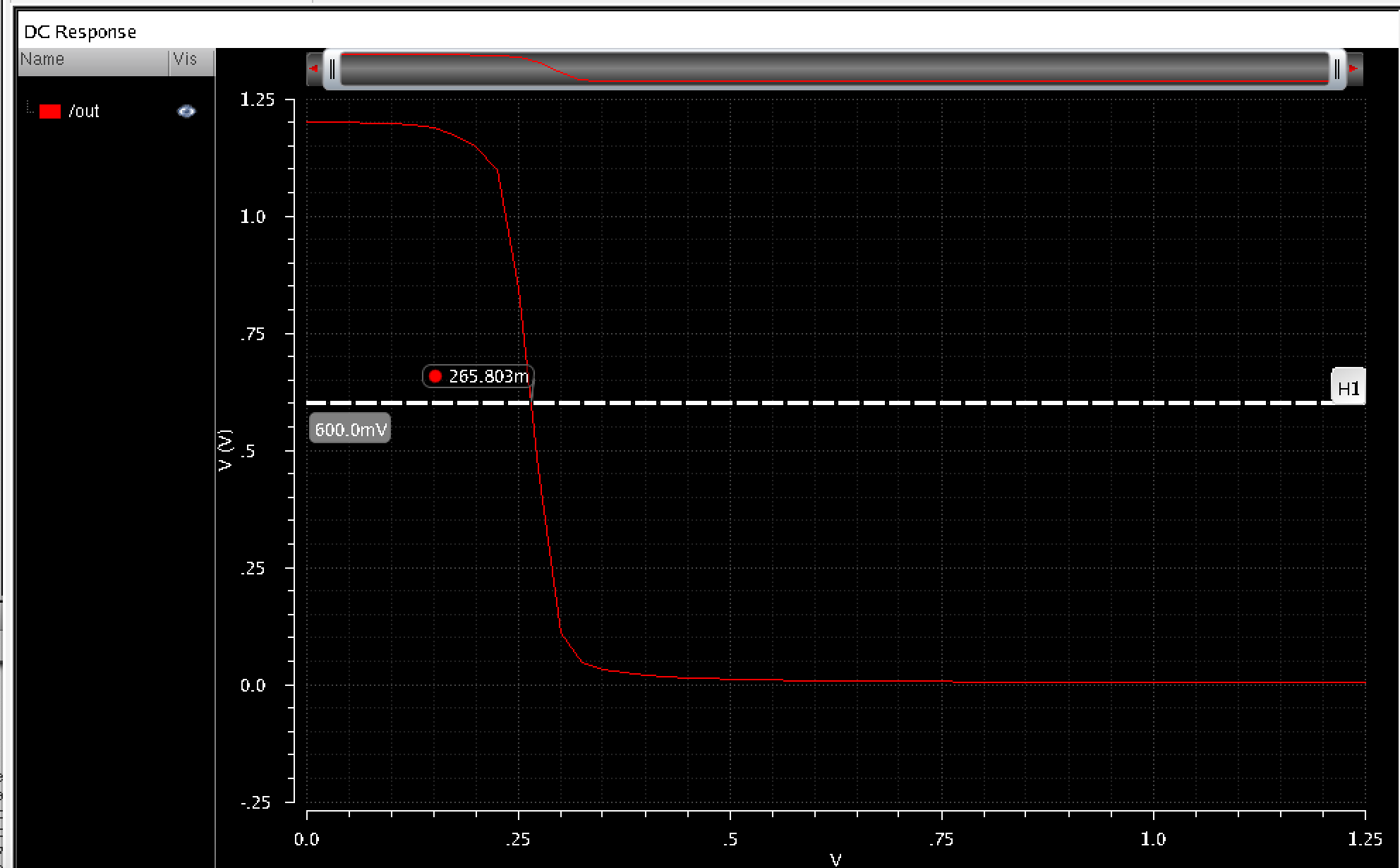
**The DC biasing of NM0 to 600mV (V DC = 600)**



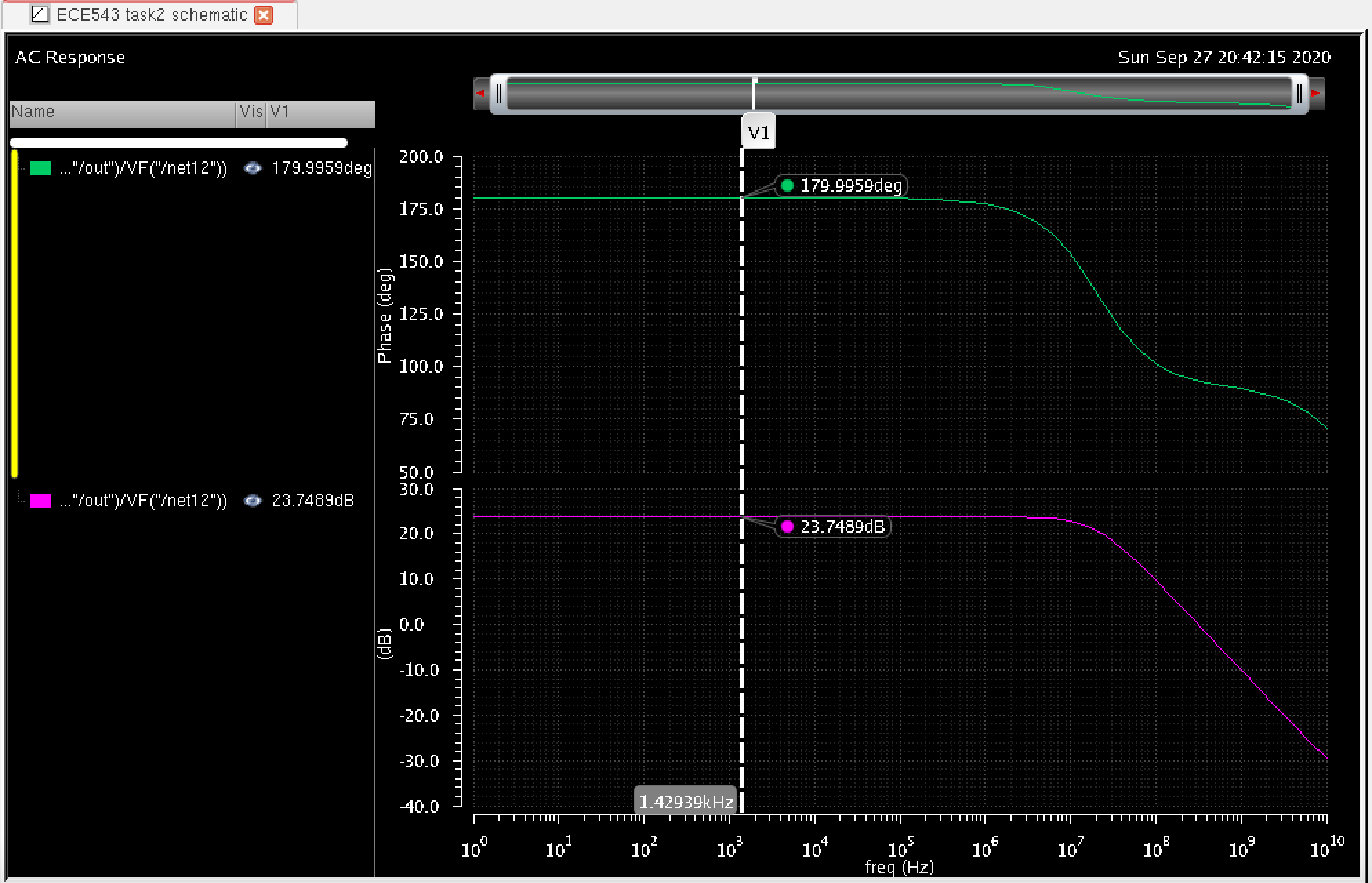
Description: After assigning the DC biasing of NMO to 600mv, we performed the AC Analysis and found out that the gain is very low as shown in the figure bellow which is almost -32.9. The gain was very low due to the decrease of signal frequency as shown in the figure below.

Part3: Performing DC sweep for V1 dc voltage to find the dc value such that the output DC value is 600mV.

**The DC biasing of NM0 to the value found in DC sweep**

Description: We performed a DC sweep for V1 dc voltage to find the dc value such that the output dc value is 600 mv and as it is shown in the figure is how we found the value of the input voltage.

**The DC Biasing of NMOS within the performance of phase and Gain of the Amplifier**

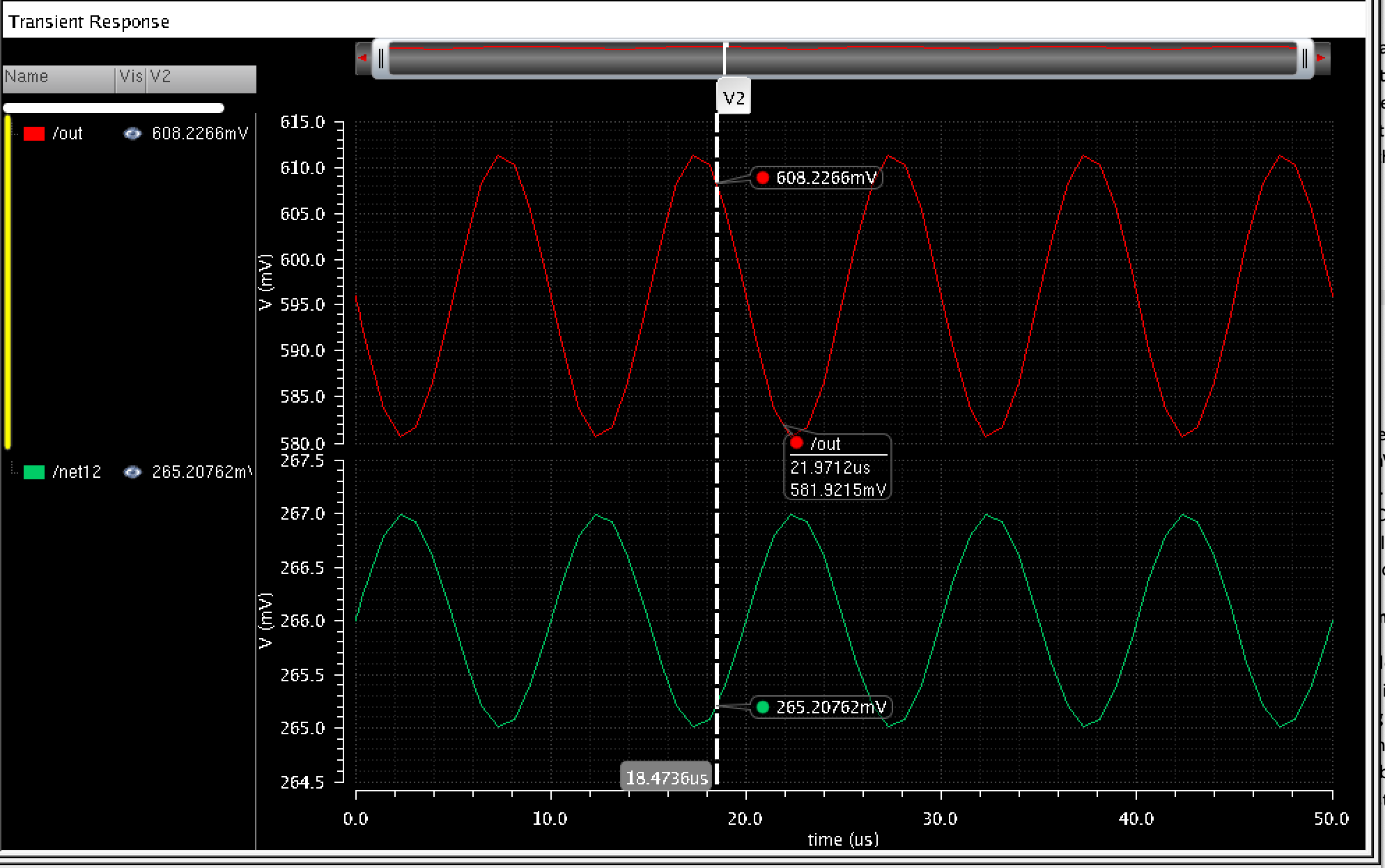


Description: The dc biasing of NMO was assigned to the value found in the dc sweep as was shown in the figure above. Also, the performance of ac analysis was used to find the gain. After running multiple tests of the NMOS performance, we discovered that when the voltage increases, the frequency increases as well. Thus causing the gain to improve faster in performance.

Part 4: Changes in V2 using Sinusoidal with DC biasing voltage

Performance:

We obtained the DC biasing voltage to change the signal of V2 to be sinusoidal signal with an amplitude of 1mv and the frequency of 1 k HZ and then performed the transient analysis to plot the amplifier output. Then we verified the gain obtained from the transient analysis that is consistent with the gain from the ac analysis form part3 as shown in the figure bellow. And then we calculated the gain from the output and input using the formula 20log Vout/Vin to be =7.2 which is low.

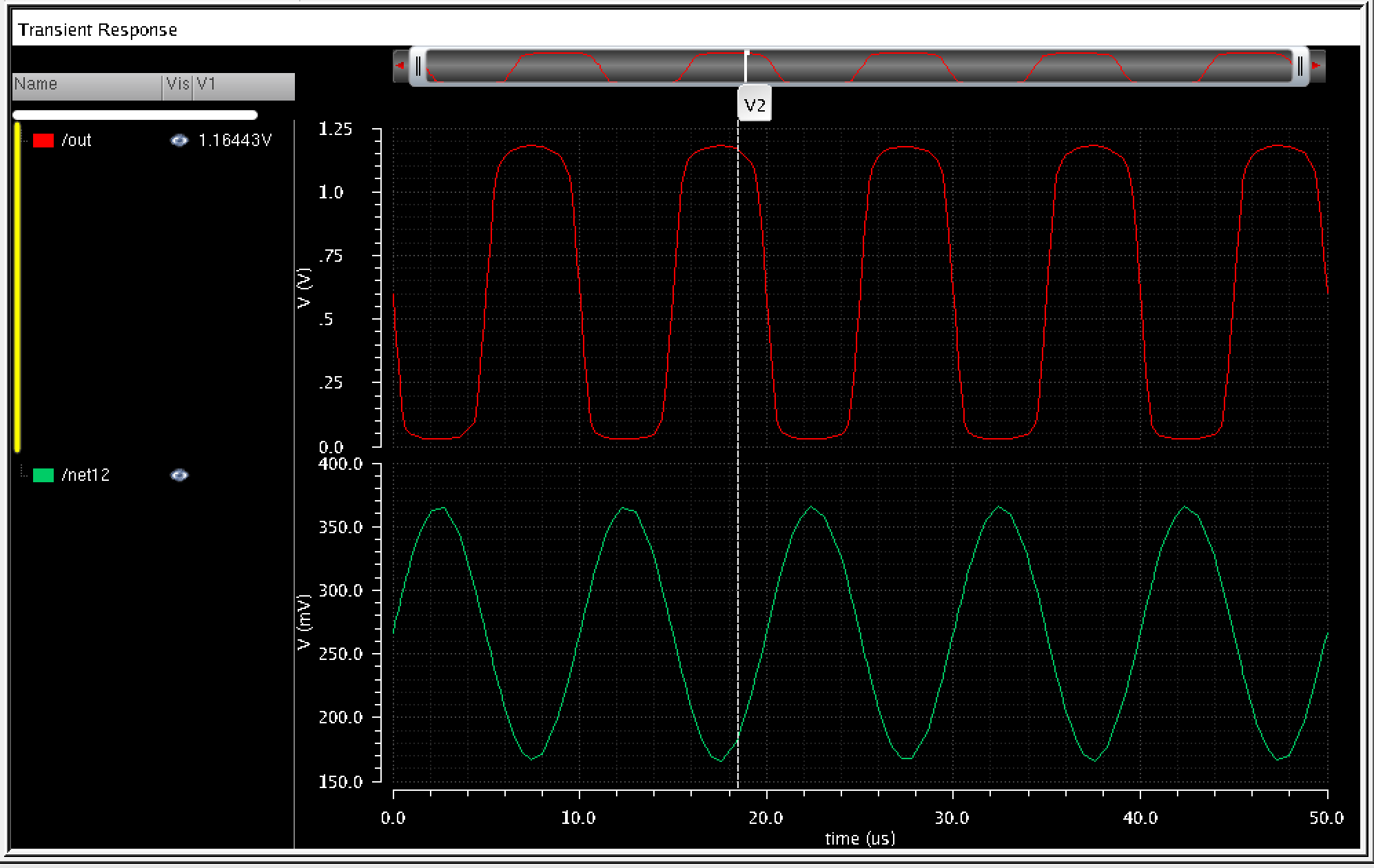


Part5: Transient Analysis

Performance:

We changed the amplitude of the sinusoidal signal to 100mv and repeated the transient analysis again and we realized that the output has changed a little bit of the amplitude of the gain if we were to calculate the gain of that signal, it would be somewhere around 16.7 which is higher than the previse one.

**Transit Analysis of Changes in the amplitude of the sinusoid**



*Conclusion:*

In this lab we learned how to perform AC and Transient analysis and how to calculate the gain from the output and input values. From becoming accustomed to using the tools in the Virtuoso program, we were able to complete our task at analyzing the behavior of common emitter amplifiers and common source amplifiers through sinusoid.